What is claimed is:

1. A surge protection device comprising:

a gate electrode embedded in an insulator;

a source electrode and a drain electrode on said insulator, the source and drain electrodes respectively forming first and second capacitances with the gate electrode; and

a semiconductor island on said insulator, the island forming a channel region between said source and drain electrodes and a third capacitance with said gate electrode, the third capacitance being smaller than either of said first and second capacitances,

said source and drain electrodes being adapted for connection to external circuitry for establishing a low-impedance path when said external circuitry is subjected to a surge potential.

2. The surge protection device of claim 1, wherein said first and second capacitances are of equal value.

3. A surge protection circuit comprising:

a plurality of surge protection devices,

each of said protection devices comprising:

a gate electrode embedded in an insulator;

a source electrode and a drain electrode on said insulator, the source and drain electrodes respectively forming first and second capacitances with the gate electrode; and

a semiconductor island on said insulator, the island forming a channel region between said source and drain electrodes and a third

capacitance with said gate electrode, the third capacitance being smaller than either of said first and second capacitances,

the source and drain electrodes of each of said surge protection devices being respectively connected to the drain and source electrodes of adjacent ones of said plurality of surge protection devices and further connected to pad electrodes of external circuitry for establishing connections with said adjacent surge protection devices when one of said pad electrodes is subjected to a surge potential.

4. The surge protection circuit of claim 3, wherein said first and second capacitances of each of said surge protection devices are of equal value.

5. The surge protection circuit of claim 3, further comprising:

a second plurality of surge protection devices identical in structure to said plurality of surge protection devices,

the source-drain paths of the second plurality of surge protection devices being respectively connected to said pad electrodes via respective lines for establishing a low-impedance path to ground.

6. The surge protection circuit of claim 3, further comprising:

a second surge protection device identical in structure to said plurality of surge protection devices and connected between a first one of said plurality of surge protection devices and ground; and

a third surge protection device identical in structure to said plurality of surge protection devices and connected between a second one of said plurality of surge protection devices and ground.

7. The surge protection circuit of claim 6, further comprising a second plurality of surge protection devices identical in structure to said plurality of surge protection devices, the source-drain paths of the second plurality of surge protection devices being respectively connected to said pad electrodes via respective lines for establishing a low-impedance path to ground.

8. A surge protection circuit comprising:

a plurality of surge protection devices,

each of said protection devices comprising:

a gate electrode embedded in an insulator;

a source electrode and a drain electrode on said insulator, the source and drain electrodes respectively forming first and second capacitances with the gate electrode; and

a semiconductor island on said insulator, the island forming a channel region between said source and drain electrodes and a third capacitance with said gate electrode, the third capacitance being smaller than either of said first and second capacitances,

the source and drain electrodes of each of said surge protection devices being connected in series to external circuitry for establishing a low-impedance path to ground when the external circuitry is subjected to a surge potential.

9. The surge protection circuit of claim 8, wherein said first and second capacitances of each of said surge protection devices are of equal value.

10. A surge protection circuit for a semiconductor display panel which includes:

a first plurality of pad electrodes;

a plurality of vertical signal lines connected respectively to said first plurality of pad electrodes;

a second plurality of pad electrodes; and

a plurality of horizontal signal lines intersecting said vertical signal lines, the horizontal signal lines being connected respectively to said second plurality of pad electrodes,

the surge protection circuit comprising a plurality of floating-gate field effect transistors, each including a floating gate electrode, a source electrode and a drain electrode, the source and drain electrodes of each of said transistors being respectively connected to the drain and source electrodes of adjacent ones of said plurality of floating-gate transistors and further connected to said first plurality of pad electrodes for establishing connections with said adjacent floating-gate transistors when one of said first plurality of pad electrodes or one of said plurality of vertical signal lines is subjected to a surge potential.

11. The surge protection circuit of claim 10, wherein the floating gate electrode of each of said floating-gate field effect transistors is embedded in an insulator and said source electrode and said drain electrode are formed on said insulator so that the source and drain electrodes respectively form first and second capacitances with the floating gate electrode and a semiconductor island is provided on said insulator to form a channel between said source and drain electrodes and a third capacitance with said

gate electrode, the third capacitance being smaller than either of said first and second capacitances.

12. The surge protection circuit of claim 10, wherein said first and second capacitances of each of said floating-gate transistors are of equal value.

13. The surge protection circuit of claim 10, further comprising a second plurality of floating-gate transistors, the source-drain paths of the second plurality of floating-gate transistors being respectively connected to said first plurality of pad electrodes via respective lines for establishing a low-impedance path to ground.

14. The surge protection circuit of claim 10, further comprising:

a second floating-gate transistor connected between a first one of said plurality of floating-gate transistors and ground; and

a third floating-gate transistor connected between second one of said plurality of floating-gate transistors and ground.

15. The surge protection circuit of claim 14, further comprising a second plurality of floating-gate transistors, the source-drain paths of the second plurality of floating-gate transistors being respectively connected to said first plurality of pad electrodes via said vertical signal lines for establishing a low-impedance path to ground.

16. A surge protection circuit for a semiconductor display panel

which includes:

a first plurality of pad electrodes;

a plurality of vertical signal lines connected respectively to said first plurality of pad electrodes;

a second plurality of pad electrodes; and

a plurality of horizontal signal lines intersecting said vertical signal lines, the horizontal signal lines being connected respectively to said second plurality of pad electrodes,

the surge protection circuit comprising a plurality of floating-gate field effect transistors, each including a floating gate electrode, a source electrode and a drain electrode, the source and drain electrodes of each of said transistors being respectively connected to said vertical signal lines for establishing a low-impedance path to ground when one of said first plurality of pad electrodes or one of said plurality of vertical signal lines is subjected to a surge potential.

17. The surge protection circuit of claim 16, wherein the floating gate electrode of each of said floating-gate field effect transistors is embedded in an insulator and said source electrode and said drain electrode are formed on said insulator so that the source and drain electrodes respectively form first and second capacitances with the floating gate electrode and a semiconductor island is provided on said insulator to form a channel between said source and drain electrodes and a third capacitance with said gate electrode, the third capacitance being smaller than either of said first and second capacitances.

18. The surge protection circuit of claim 17, wherein said first and second capacitances of each of said floating-gate transistors are of equal value.